Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A data processing device, ~~capable of decoding and executing~~ which decodes and executes instructions containing a spare field, comprising:

~~a~~ an instruction cache ~~memory where said instructions are held,~~ memory; ~~wherein said instructions each contain a spare field, and~~

~~wherein said cache memory holds information which is generated according to predecoding of instructions in a first corresponding area corresponding to said spare field~~

a predecode-processor which decodes operation codes contained in first fields of each of said instructions to generate a piece of information, said information representing whether said instruction is a branch instruction or not, and transfers the information as said spare field of each of said instructions; and

an instruction flow unit which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory.

wherein the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that said instruction is a branch instruction according to said information of the said spare field.

2. – 7. (canceled)

8. (currently amended) The data processing device according to ~~claim 7~~claim 1, ~~further comprising~~:

wherein the instruction flow unit comprises:

a queuing buffer temporarily storing instructions loaded from said instruction cache memory; and

a target buffer which holds an address of said ~~branched place~~branch destination, said instruction of said ~~branched place~~branch destination, and a following address of said address of said ~~branched place~~branch destination,

wherein said ~~controlling means~~ instruction flow unit divides one branch operation into a prepare target instruction and a branch procedure instruction,

wherein said prepare target instruction commands ~~the calculations~~ calculating of said address of said ~~branched place~~ branch destination and fetching of said instruction of said ~~branched place~~branch destination,

wherein said branch procedure instruction commands branch condition checks and branch procedures.

9. (currently amended) The data processing device according to claim 8,

wherein said ~~controlling means~~ instruction flow unit issues commands to load said instruction of said ~~branched place~~ branch destination and said following address from said target buffer when said ~~controlling means~~ instruction flow unit determines that said instruction is a branch procedure instruction according to said information of said queuing buffer ~~which was loaded from first corresponding area of said cache memory~~.

10. – 11. (canceled)

12. (currently amended) The data processing device according to ~~claim 10~~claim 1,

wherein to handle relative branch instructions of program counters with n bit displacements, said ~~processor~~ predecode-processor adds information of n lower bits of addresses of said program counters for displacements of said first fields in an adding operation, and

~~wherein added results by said processor are held in said second corresponding area of said cache memory, and~~

wherein carry information of said adding operation is held in ~~said first corresponding area~~ said spare field of each of said instructions.

13. – 20. (canceled)